PXI8191
User's Manual

Beijing ART Technology Development Co., Ltd.

Table of Contents

FEATURES

Analog Input

- AD converter type: AD7663(default), AD7665
- Input Range: ±10V,±5V, ±2.5V, 0~10V, 0~5V
- 16-bit resolution
- Sampling Rate: 250KHz (max) (500KHz when using AD7665)
- Input channel: 32SE/16DI
- Isolated voltage: 2500Vrms (1 min)
- Data Read Mode: software inquiry, non-empty and half-full mode
- FIFO Size: 8K word
- Memory Sign: non-empty, half-full, full (overflow)
- Sample mode: continuous sampling, group sampling
- Group Interval: software-configurable, minimum value is sapling period, maximum value is 419400μS
- Clock Source: internal clock and external clock
- Trigger Mode: software trigger and hardware trigger
- Trigger Type: edge trigger and level trigger
- DTR range: TTL
- Trigger Direction: negative, positive, either positive or negative trigger
- Analog input impedance: 10MΩ
- Non-linear error: ±3LSB(Maximum)
- System Measurement Accuracy: 0.01%
- Operating Temperature Range: 0℃~+55℃
- Storage Temperature Range: -20℃~+70℃

Chapter 1 Overview

ART PXI8191 module is designed for data acquisition applications with 16-bit resolution analog input.

It can be directly inserted into IBM-PC/AT or a computer which is compatible with PXI8191 to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Unpacking Checklist

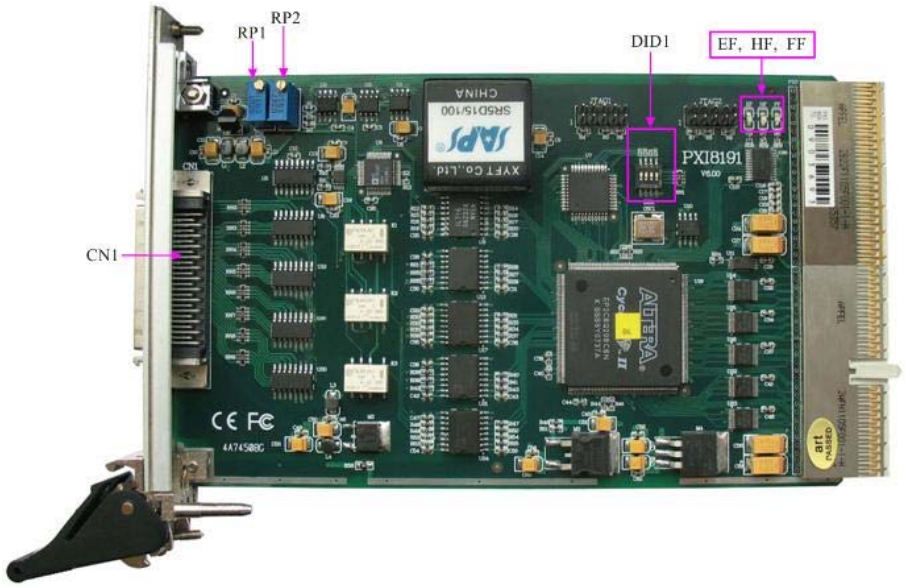
Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.

Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- PXI191 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

Chapter 2 Component Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram



2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

CN1: Analog signal input and output connectors

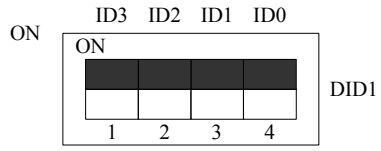
2.2.3 Potentiometer

RP1: Analog input zero-point adjustment potentiometer
RP2: Analog input full-scale adjustment potentiometer

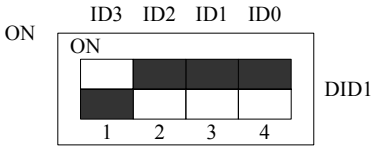
2.2.3 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one PXI8191, you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following four-bit number is expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: "ID3" is the high bit."ID0" is the low bit, and the black part in the diagram represents the location of the switch. (Test software of the company often uses the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible. As for the

differences between logic ID and physical ID, please refer to the function explanations of "CreateDevice" and "CreateDeviceEx" of ***The Prototype Explanation of Device Object Management Function*** in ***PXI8191S*** software specification).



The above chart shows"1111", so it means that the physical ID is 15.



The above chart shows"0111", so it means that the physical ID is 7.

The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	物理ID（Hex）	物理ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1
OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

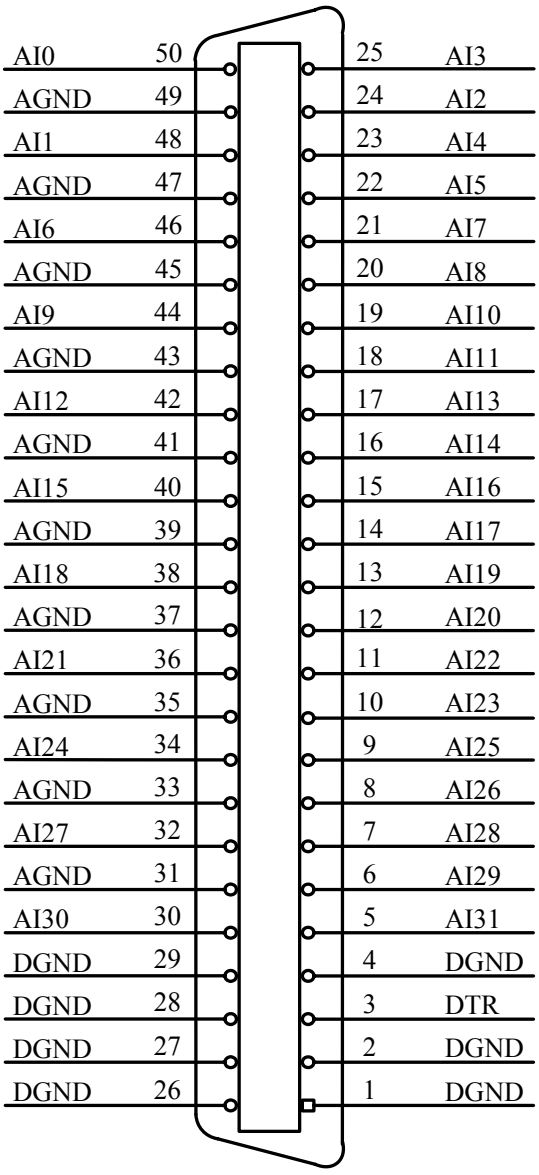
2.2.4 Status indicator

EF: FIFO non-empty status indicator
HF: FIFO half-full status indicator
FF: FIFO overflow status indicator

Chapter 3 Signal Connectors

3.1 The Definition of Signal Input and Output Connectors

50 core plug on the CN1 pin definition

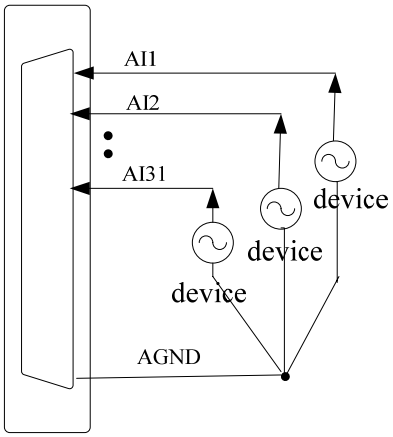


Pin Name	Dir	Description
AI0-AI31	Input	Analog input, reference ground is AGND.
AGND	GND	Analog ground.
DGND	GND	Digital ground.
DTR	Input	Digital trigger signal, reference ground is DGND.

Chapter 4 Connection Ways for Each Signal

4.1 Analog single-ended input

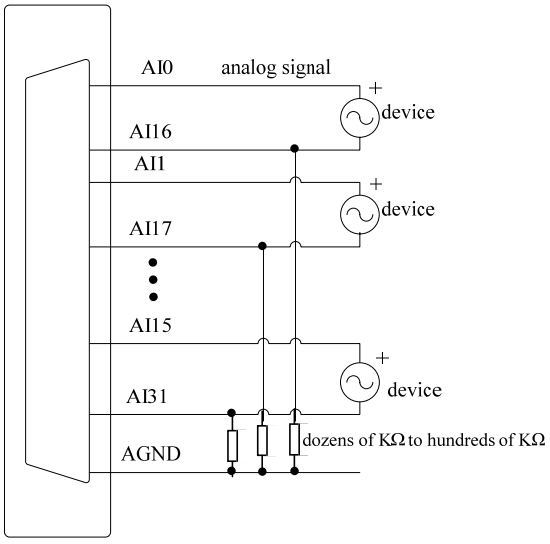
Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.



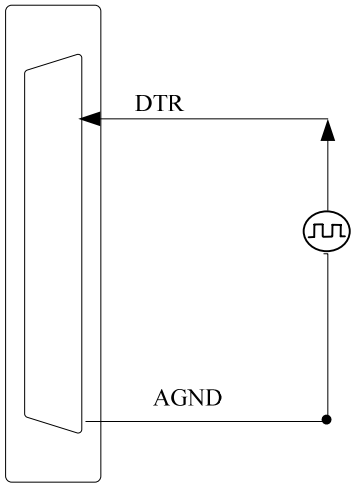
4.2 Analog differential inputs

Double-ended input mode, which was also called differential input mode, uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to PXI8191 software manual.

According to the diagram below, PXI8191 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 16-channel analog input signal is connected to AI0~AI15, the negative side of the analog input signal is connected to AI16~AI31, equipments in industrial sites share the AGND with PXI8191 board.

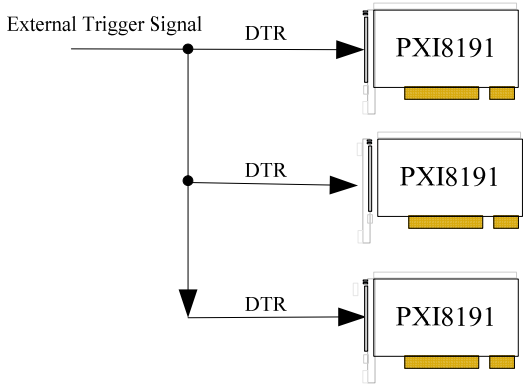


4.2 Trigger signal input



4.4 Realization of the Multi-Card Synchronization

When using the common external trigger to achieve multi-card synchronization, please make sure all parameters of different PXI8191 are the same. At first, configure hardware parameters, and use analog trigger signal (ATR), then connect the signal that will be sampled by PXI8191, input triggering signal from DTR pin, then click “Start” button, at this time, PXI8191 does not sample any signal but waits for external trigger signal. When each module is waiting for external trigger signal, use the common external trigger signal to startup modules, at last, we can realize synchronization data acquisition in this way. See the following figure:



Chapter 4 The Instruction Trigger Function

4.1 Internal Trigger Mode

When A/D is in the initialization, if the hardware parameter ADPara.TriggerMode = PXI8191_TRIGMODE_SOFT, we can achieve the internal trigger acquisition. In this function, when calling the StartDeviceProAD function, it will generate A/D start pulse, A/D immediately access to the conversion process and not wait for the conditions of any other external hardware. It also can be interpreted as the software trigger.

As for the specific process, please see the figure below, the cycle of the A/D work pulse is decided by the sampling frequency.

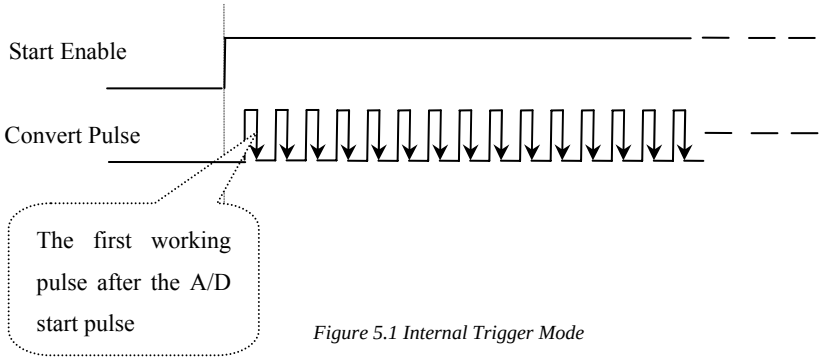


Figure 5.1 Internal Trigger Mode

4.2 External Trigger Mode

When A/D is in the initialization, if the hardware parameter ADPara.TriggerMode = PXI8191_TRIGMODE_POST, we can achieve the external trigger acquisition. In this function, when calling the StartDeviceProAD function, A/D will not immediately access to the conversion process but wait for the external trigger source signals accord with the condition, then start converting the data. It also can be interpreted as the hardware trigger. Trigger source is DTR.

The trigger modes include the edge trigger and level trigger.

(1) Edge trigger function

Edge trigger is to capture the characteristics of the changes between the trigger source signal and the trigger level signal to trigger A/D conversion.
When TriggerType = PXI8191_TRIGTYPE_EDGE, it is dege trigger.
When ADPara.TriggerDir = PXI8191_TRIGDIR_NEGATIVE, choose the trigger mode as the falling edge trigger. That is, when the trigger signal is on the falling edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition.

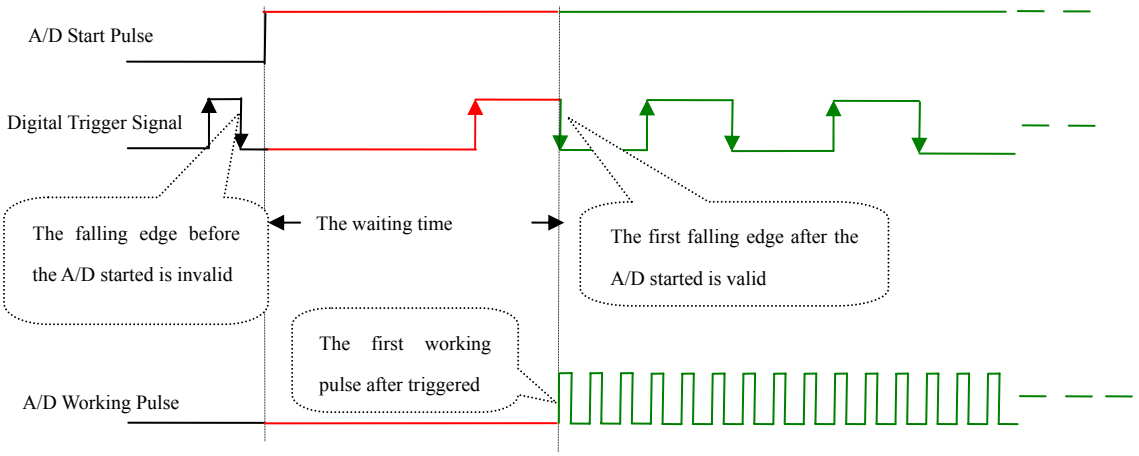


Figure5.2 Digital Trigger Source，Falling edge Trigger

When ADPara.TriggerDir = PXI8191_TRIGDIR_POSITIVE, choose the trigger mode as rising edge trigger. That is, when the trigger signal is on the rising edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition.

When ADPara.TriggerDir = PXI8191_TRIGDIR_POSIT_NEGAT, choose the trigger mode as “either rising or falling edge trigger”. That is, when the trigger signal is on the rising or falling edge, A/D will immediately access to the conversion process, and its follow-up changes have no effect on A/D acquisition. This function can be used in the case that the acquisition will occur if the **exoteric** signal changes.

（2）Level trigger function

Level trigger is to capture the condition that trigger signal is higher or lower than the trigger level to trigger AD conversion.
When ADPara.TriggerType = PXI8191_TRIGTYPE_PULSE, it is level trigger.
When ADPara.TriggerDir = PXI8191_TRIGDIR_ NEGATIVE, it means the trigger level is low. When trigger signal is low level, AD is in the conversion process, once the trigger signal is in the high level, A/D conversion will automatically stop, when the trigger signal is in the low level again, A/D will re-access to the conversion process that is, only converting the data when the trigger signal is in the low level.

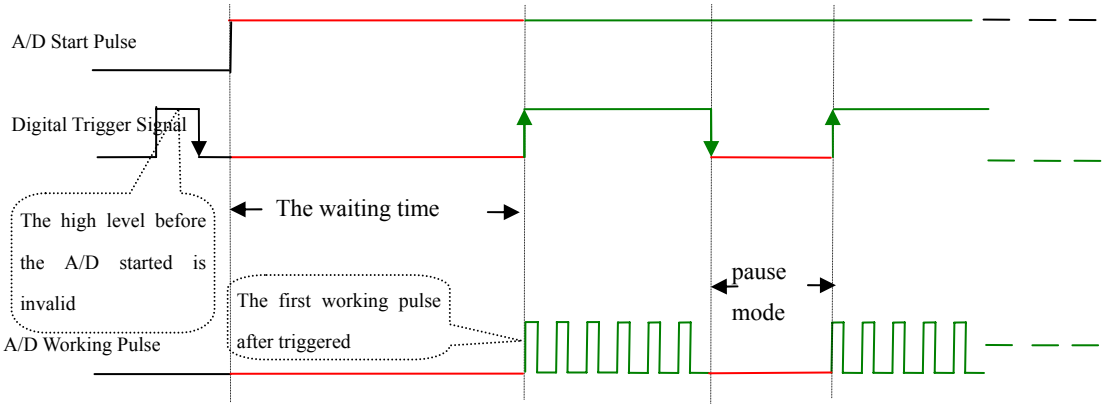


Figure5.4 Digital Trigger Source，High Level Trigger

When ADPara.TriggerDir = PXI8191_TRIGDIR_POSITIVE, it means the trigger level is high. When trigger signal is in high level, A/D is in the conversion process, once the trigger signal is in the low level, A/D conversion will automatically stop, when the trigger signal is in the high level again, A/D will re-access to the conversion process, that is, only converting the data when the trigger signal is in the high level.

When ADPara.TriggerDir = PXI8191_TRIGDIR_POSIT_NEGAT, it means the trigger level is low. The effect is the same as choosing the internal software trigger.

Chapter 5 Methods of Using Internal and External Clock Function

5.1 Internal Clock Function

Internal Clock Function refers to the use of on-board clock oscillator and the clock signals which are produced by the user-specified frequency to trigger the A/D conversion regularly. To use the clock function, the hardware parameters ADPara.ClockSource=PXI8191 _CLOCKSRC_IN should be installed in the software. The frequency of the clock in the software depends on the hardware parameters ADPara.Frequency. For example, if Frequency = 100000, that means A/D work frequency is 100000Hz (that is, 100 KHz, 10μs /point).

5.2 External Clock Function

External Clock Function refers to the use of the outside clock signals to trigger the A/D conversion regularly. The clock signals are provide by the CLKIN pin of the CN1 connector. The outside clock can be provided by PCI8301 clock output (CLKOUT of CN2), as well as other equipments, for example clock frequency generators. To use the external clock function, the hardware parameters ADPara.ClockSource = PXI8191_CLOCKSRC_OUT should be installed in the software. The clock frequency depends on the frequency of the external clock, and the clock frequency on-board (that is, the frequency depends on the hardware parameters ADPara.Frequency) only functions in the packet acquisition mode and its sampling frequency of the A/D is fully controlled by the external clock frequency.

5.3 Methods of Using Continuum and Grouping Sampling Function

5.3.1 Continuum Sampling Function

The continuous acquisition function means the sampling periods for every two data points are completely equal in the sampling process of A/D, that is, completely uniform speed acquisition, without any pause, so we call that continuous acquisition.

To use the continuous acquisition function, the hardware parameters ADPara.ADMode = PXI8191 _ADMODE_SEQUENCE should be installed in the software. For example, in the internal clock mode, hardware parameters ADPara.Frequency = 100000 (100KHz) should be installed, and 10 microseconds after the AD converts the first data point, the second data point conversion starts, and then 10 microseconds later the third data point begins to convert, and so on.

5.3.2 Grouping Sampling Function

Grouping acquisition (pseudo-synchronous acquisition) function refers to the sampling clock frequency conversion among the channels of the group in the AD sampling process, and also a certain waiting time exists between every two groups, this period of time is known as the Group Interval. Loops of group refer to numbers of the cycle acquisition for

each channel in the same group. In the internal clock mode and the fixed-frequency external clock mode, the time between the groups is known as group cycle. The conversion process of this acquisition mode as follows: a short time stop after the channels conversion in the group (that is, Group Interval), and then converting the next group, followed by repeated operations in order, so we call it grouping acquisition.

The purpose of the application of the grouping acquisition is that: at a relatively slow frequency, to ensure that all of the time difference between channels to become smaller in order to make the phase difference become smaller, thus to ensure the synchronization of the channels, so we also say it is the pseudo-synchronous acquisition function. In a group, the higher the sampling frequency is, the longer Group Interval is, and the better the relative synchronization signal is. The sampling frequency in a group depends on ADPara. Frequency, Loops of group depends on ADPara.LoopsOfGroup, the Group Interval depend on ADPara. Group Interval.

Based on the grouping function, it can be divided into the internal clock mode and the external clock mode. Under the internal clock mode, the group cycle is decided by the internal clock sampling period, the total number of sampling channels, Loops of group and Group Interval together. In each cycle of a group, AD only collects a set of data. Under the external clock mode, external clock cycle ≥ internal clock sampling cycle × the total number of sampling channels × Loops of group + AD chip conversion time, AD data acquisition is controlled and triggered by external clock. The external clock mode is divided into fixed frequency external clock mode and unfixed frequency external clock mode. Under the fixed frequency external clock mode, the group cycle is the sampling period of the external clock.

The formula for calculating the external signal frequency is as follows:

Under the internal clock mode:
Group Cycle = the internal clock sampling period × the total number of sample channels × Loops of group + AD chips conversion time + Group Interval
External signal cycle = (cycle signal points / Loops of group) × Group Cycle
External signal frequency = 1 / external signal cycle

Under the external clock mode: (a fixed-frequency external clock)
Group Cycle = external clock cycle
External signal cycle = (cycle signal points / Loops of group) × Group Cycle
External signal frequency = 1 / external signal cycle

Formula Notes:
The internal sampling clock cycle = 1 / (AD Para. Frequency)
The total number of sampling channels = AD Para. Last Channel – AD Para. First Channel + 1
Loops of group == ADPara.LoopsOfGroup
AD Chips conversion time = see "AD Analog Input Function" parameter
Group Interval = AD Para. Group Interval
Signal Cycle Points = with the display of the waveform signal in test procedures, we can use the mouse to measure the signal cycle points.

Under the internal clock mode, for example, sample two-channel 0, 1, and then 0 and 1 become a group. Sampling frequency (Frequency) = 100000Hz (cycle is 10μs), Loops of group is 1, Group Interval = 50μs, then the acquisition process is to collect a set of data first, including a data of channel 0 and a data of channel 1. We need 10μs to sample the two data, 20μs to convert the data from the two channels. After the conversion time of an AD chip, AD will automatically cut-off to enter into the waiting state until the 50μs group interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

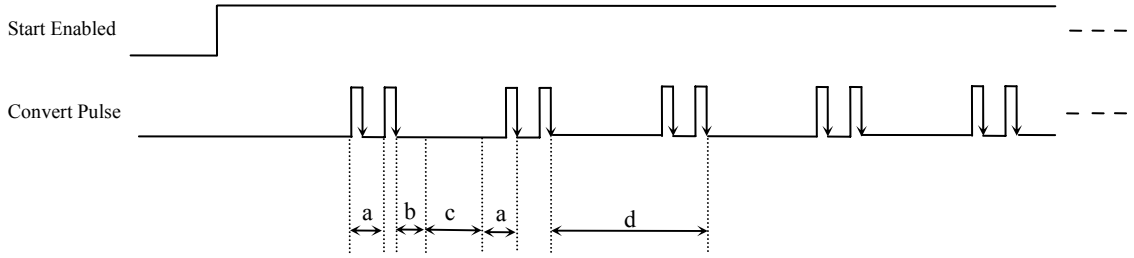


Figure5.1 Grouping Sampling which grouping cycle No is 1 under the Internal Clock Mode

Note: a— internal clock sample cycle
b— AD chips conversion time
c—Group Interval
d— group cycle

Change the loops of group into 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the conversion order is 0,1,0,1. We need 10μs to sample each of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the 50μs Group Interval ends. We start the next group, begin to convert the data of channel 0 and 1, and then enter into the waiting state again, and the conversion is going on in this way, as the diagram following shows:

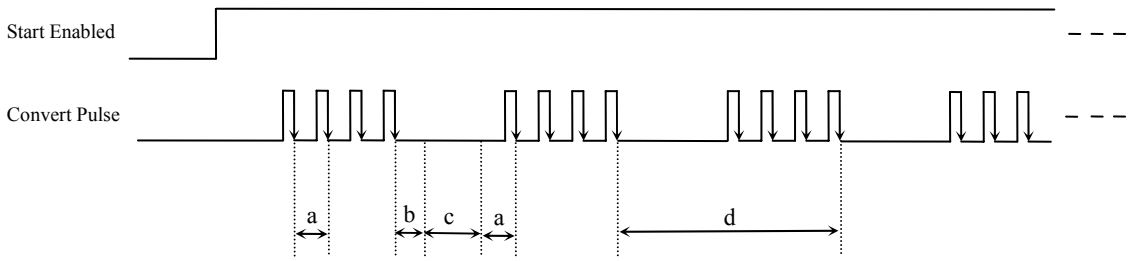


Figure 5.2 Grouping Sampling which grouping cycle No is 2 under the Internal Clock Mode

Notes: a— internal clock sample cycle
b— AD chips conversion time
c—Group Interval
d— group cycle

Under the external clock mode, the requirement is: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels× Loops of group + AD chip conversion time, otherwise, the external clock

appearing in the group conversion time will be ignored.

Under the fixed-frequency external clock mode, for example, when sampling data of two-channel 0, 1, then channel 0 and channel 1 consist of a group. Sampling frequency (Frequency) = 100000Hz (the cycle is 10μs), Loops of group is 2, then the acquisition process is to collect the first set of data, including two data of channel 0 and two data of channel 1, the order of conversion 0,1,0,1, We need 10μs to sample the four data and 40μs to convert of the four data. After the conversion time of an AD chip, AD will automatically stop to enter into the waiting state until the next edge of the external clock triggers AD to do the next acquisition, and the conversion is going on in this way, as the diagram following shows:

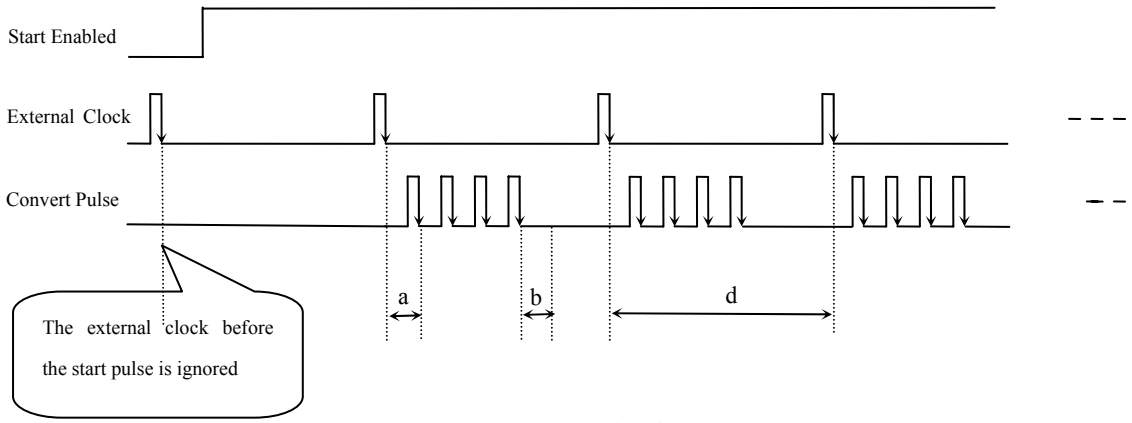


Figure 5.3 Grouping sampling under the fixed frequency external clock mode

Notes: a— internal clock sample cycle
b—AD chips conversion time
d—group cycle（external clock cycle）

Under an unfixed-frequency external clock mode, for example, the grouping sampling principle is the same as that of the fixed-frequency external clock mode. Under this mode, users can control any channel and any number of data. Users will connect the control signals with the clock input of the card (CLKIN), set the sampling channels and Loops of group. When there are external clock signals, it will sample the data which is set by users. Because the external clock frequency is not fixed, the size of external clock cycle is inconsistent but to meet: the external clock cycle ≥ the internal clock sampling period × the total number of sampling channels × Loops of group + AD chip conversion time, , otherwise, the external clock edge appearing in the group conversion time will be ignored.

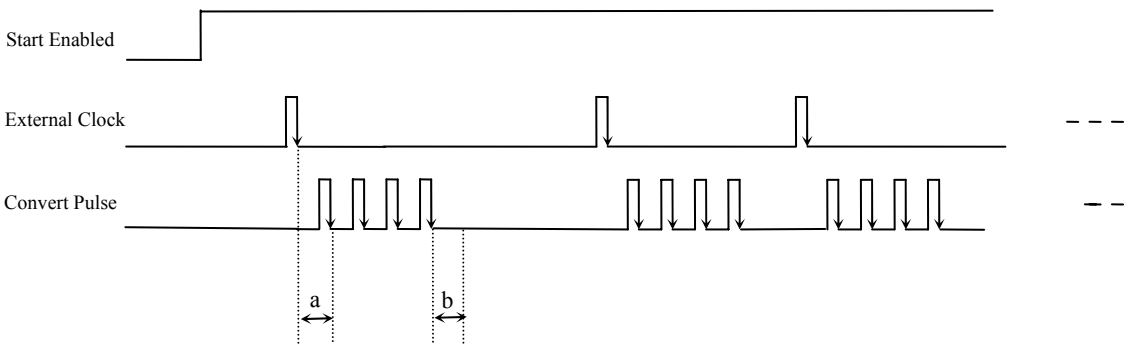


Figure 5.4 Grouping sampling under the not fixed frequency external clock mode

Note: a— internal clock sample cycle
b—AD chips conversion time

Chapter 6 Notes, Calibration and Warranty Policy

6.1 Notes:

In product's pack, user can find this user manual, PXI8191 module and quality guarantee card. Users must save quality guarantee card carefully, if the products have some problems and need for repair, please send products together with quality guarantee card to ART, we will make very good after-sale service and solve the problem as quickly as we can.

When using PXI8191, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of PXI8191 module.

6.2 Calibration

Every device has been calibrated before leaves the factory. After using for a period of time or change the set of the input range, in this case, user needs to calibrate the module. PXI8191 default input range: ±5V, in this manual, we introduce how to calibrate PXI8191 in ±5V input range; other input range calibration is the same as ±5V.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the PXI8191 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take channel AI0+ for example, put 0V into AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±5V input range and start sampling, adjust potentiometer RP1 in order to make voltage value is 0.000V or near 0.000V. Other channels zero adjustment is the same as this one.
2) Full-scale adjustment: select one channel of analog inputs, take channel AI0 for example, put 5V into AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±5V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 4999.84mV or near 4999.84mV. Other channels full-scale adjustment is the same as this one.
3) Repeat steps heretofore, until meet the requirement.

6.3 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly.
2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:
- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.